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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/519,175      | 12/20/2004  | Kouta Nagano         | 16869S-137100US     | 5251             |

7590 09/06/2005

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|          |
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| EXAMINER |
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HARRISON, MONICA D

|          |              |
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| ART UNIT | PAPER NUMBER |
|----------|--------------|

2813

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/519,175

Applicant(s)

NAGANO ET AL. 

Examiner

Monica D. Harrison

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9 and 11-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Atsuo et al (JP 2002-9111A).

1. Regarding claim 1, Atsuo et al discloses a producing method of a semiconductor device, characterized by including a step (b) in which a thermosetting resin is baked at temperature higher than a resin sealing temperature of a step after the step which the thermosetting resin is thermally cured to seal a semiconductor chip with resin (pp.5-6, paragraphs 0014-0021).

2. Regarding claim 2, Atsuo et al discloses in that the (b) step is a step in which the curing the thermosetting resin is advanced (pp.5-6, paragraphs 0014-0021).

3. Regarding claim 3, Atsuo et al discloses that the (b) step is performed at 220-260C (pg.6, paragraph 0020).

4. Regarding claim 4, Atsuo et al discloses further including a step (c) in which a characteristic of the semiconductor chip is inspected, after said step (b) (pp.5-6, paragraphs 0014-0021).

5. Regarding claim 5, Atsuo et al discloses that the semiconductor chip is an integrated circuit (Drawing 1, reference 19).

6. Regarding claim 9, Atsuo et al discloses a producing method of a semiconductor device, characterized by including a step in which a thermosetting resin is thermally cured to seal a semiconductor chip (Drawing 1, reference 22) and a lead (Drawing 1, reference 14) electrically connected to an electrode (Drawing 1, reference 21) of a main surface of the semiconductor chip with the resin, a step (b) in which the thermosetting resin is baked at a temperature higher than the resin sealing temperature in the step (a) after said step (a) and a step (c) in which a characteristic of the semiconductor chip is inspected after said step (b) (pp.5-6, paragraphs 0014-0021).1

7. Regarding claim 11, Atsuo et al discloses that the lead is adhesively fixed to the main surface of the semiconductor chip (Drawing 1, reference 14).

8. Regarding claim 12, Atsuo et al discloses that the lead is arranged at a periphery of the semiconductor chip (Drawing 1, reference 14).

9. Regarding claim 13, Atsuo et al discloses that the electrode of the semiconductor chip is electrically connected to the lead through a protruding electrode (Drawing 1, reference 20).

10. Regarding claim 14, Atsuo et al discloses a producing method of a semiconductor device characterized by including a step (a) in which a thermosetting resin is cured to seal with the resin the semiconductor chip mounted on a wiring substrate, a step (b) in which the thermosetting resin is baked at a temperature higher than the resin sealing temperature in the step

Art Unit: 2813

(a) after the step (a) and a step (c) in which characteristic of the semiconductor chip is inspected after the step (b) (Drawing 1, pp.5-6; paragraphs 0014-0021).

11. Regarding claim 15, Atsuo et al discloses a producing method of an electronic apparatus, characterized by including a step of preparing a semiconductor device produced by a producing method including a step in which, after a step in which a thermosetting resin is cured to seal a semiconductor chip with the resin and before a step in which a characteristic of the semiconductor chip is inspected, the thermosetting resin is baked at a temperature higher than the resin sealing temperature in said resin sealing step, and a step in which the semiconductor device is mounted on a substrate with a solder (pp.5-6, paragraphs 0014-0021).

12. Regarding claim 16, Atsuo et al discloses that the mounting step is performed with Pb-free solder (pg.5, paragraph 0017 *Au ball bump*).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsuo et al (JP 2002-9111A) in view of Bolken et al (6,576,496 B1).

13. Atsuo et al discloses all above claimed subject matter except a transfer molding process (claim 6), potting process (claim 7), the temperature changes of the thermosetting resin (claim 8), and the bonding wire (claim 10).

Bolken et al discloses a transfer molding process (column 2, lines 46-68 thru 1-13), potting process (column 2, lines 26-62), the temperature changes of the thermosetting resin (column 13, lines 4-10), and the bonding wire (Figure 1A, reference 24).

Since Atsuo et al and Bolken et al are both from the same field of endeavor, the purpose disclosed by Bolken et al would have been recognized as the pertinent art of Atsuo et al.


It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Atsuo et al with the teachings of Bolken et al, for the purpose of providing an encapsulating method and apparatus that allows high throughput production of reliable semiconductor die packages.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Application/Control Number: 10/519,175

Page 6

Art Unit: 2813

Monica D. Harrison  
AU 2813

mdh  
September 1, 2005